MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2018/2019

EEN1046 – ELECTRONICS III

(TE / RE)

31 MAY 2019
9:00 a.m. - 11:00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

(a) This booklet consists of 7 pages including cover pages with 4 questions only.

(b) Attempt **ALL** questions given. All questions carry equal marks and distribution of the marks for each question is given.

(c) Please write all your answers in the Answer Booklet provided.

(d) All necessary working **MUST** be shown.

Question 1

(a) List all SIX characteristics of an ideal operational amplifier. [6 marks]

(b) A four input (V_{IN1}, V_{IN2}, V_{IN3}, and V_{IN4}) ideal op-amp circuit with feedback resistor (R_f) and input resistors (R_1, R_2, R_3, and R_4) is shown in Figure Q1(b).

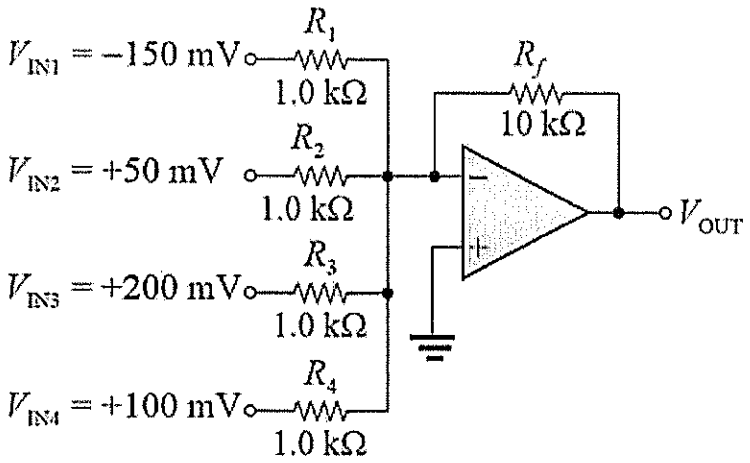

Figure Q1(b)

(i) Derive the expression for V_{OUT} in terms of V_{IN1}, V_{IN2}, V_{IN3}, and V_{IN4}. [6 marks]

(ii) Based on your answer in Q1(b)(i), determine the output voltage, V_{OUT}. [2 marks]

(iii) Name the amplifier circuit in Figure Q1(b) and suggest the usage of this amplifier circuit by giving an example of its practical application. [6 marks]

(c) Explain the concept of virtual ground in an ideal operational amplifier circuit. [5 marks]

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Question 2

(a) Determine the cutoff frequency, of a Butterworth high-pass filter with 3 poles, if its gain magnitude is 40dB below its maximum value at 1.5 kHz. [4 marks]

(b) As a circuit design engineer, you are required to design a series regulator, in order to regulate the output voltage of an unregulated power supply. The regulator must be based on a Zener diode and a bipolar junction transistor (BJT). The source voltage, V_S, is 16 V. The Zener diode employed in the regulator has a Zener knee current, I_{ZK}, of 11 mA. The BJT has an amplification factor, h_{FE}, of 130. The resistor, R, employed in the series regulator is 1.5 kΩ. The load can be represented by a 250 Ω resistor. Your series regulator designs should be able to provide a regulated output voltage (V_O) of 8 V.

(i) Sketch your design for this series regulator, and label all the components. [3 marks]

(ii) Determine the input and output power, and the wasted power dissipation in the series regulator. [5 marks]

(iii) Calculate the efficiency of the series regulator. [2 marks]

(c) Describe the required conditions for a sinusoidal oscillator to sustain oscillation. [2 marks]

(d) A Wein-Bridge oscillator is shown in Figure Q2(d). If the value of capacitor C is 0.01 μF and the value of resistor R_1 is 4.7 kΩ, design the Wein-Bridge oscillator for an oscillation frequency of 5 kHz. Determine the following:

(i) Feedback factor at oscillation frequency. [3 marks]

(ii) The resistance R of the Wein bridge oscillator. [3 marks]

(iii) The resistance R_2. [3 marks]

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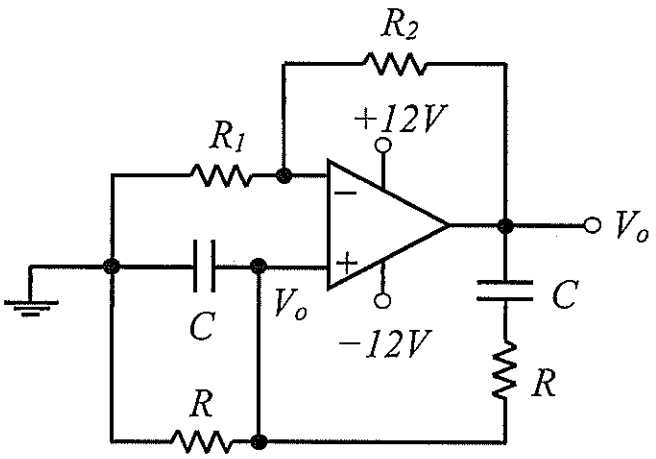

Figure Q2(d)

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Question 3

(a) A practical operational amplifier provides high gain from dc up to a given frequency, beyond which some limitations will arise. State the limitation and the closed loop circuit characteristics affected by the limitations. [4 marks]

(b) Consider a non-ideal operational amplifier circuit as shown in Figure Q3(b). The power supply given is ± 8 V.

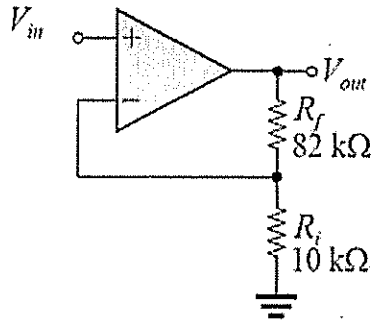

Figure Q3(b)

(i) Is this an inverting or a non-inverting amplifier circuit? [1 mark]

(ii) Calculate the maximum frequency supported by the circuit if a load resistor (R_L = 6 kΩ) is added to the circuit. The slew rate of the amplifier is 0.5 V/μs. [3 marks]

(iii) Hence, find the maximum peak input voltage allowable. [4 marks]

(iv) Define slew rate. With the aid of a diagram, explain what will happen to the output of the circuit if the input exceeds the given slew rate. [2+4 marks]

(c) Figure Q3(c) is an equivalent circuit of a practical non-inverting amplifier.

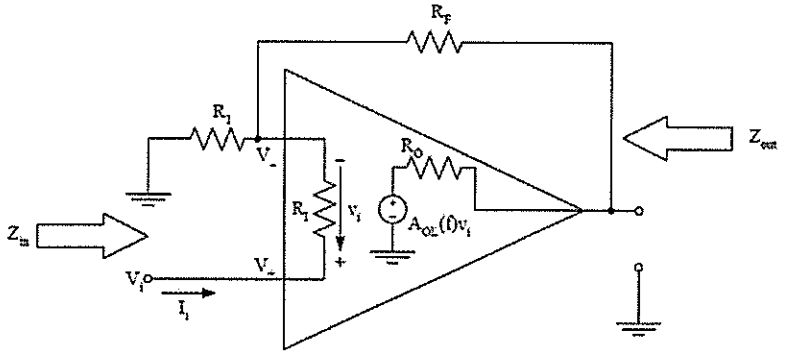

Figure Q3(c)

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Based on Figure Q3(c), prove that the output impedance, Z_{out}, can be approximated as $R_o \frac{R_F}{R_1(A_{OL})}$ where R_o is the output resistor, R_1 is the input resistor, R_F is the feedback resistor, and A_{OL} is the open-loop voltage gain. Discard the bias current, offset current, and offset voltage when deriving Z_{out}. [7 marks]

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Question 4

(a) Draw the diagram of a simple precision clamping circuit and explain its operation with the help of waveforms. [5 marks]

(b) v_a, v_b and v_c are three analog voltage signals. Design a circuit whose output is $2v_a + 3v_bv_c$ with the help of operational amplifiers and other necessary components as necessary. [8 marks]

(c) A voltage, V_{in} is connected to the inverting input of a precision clamper as shown in Figure Q4(c).

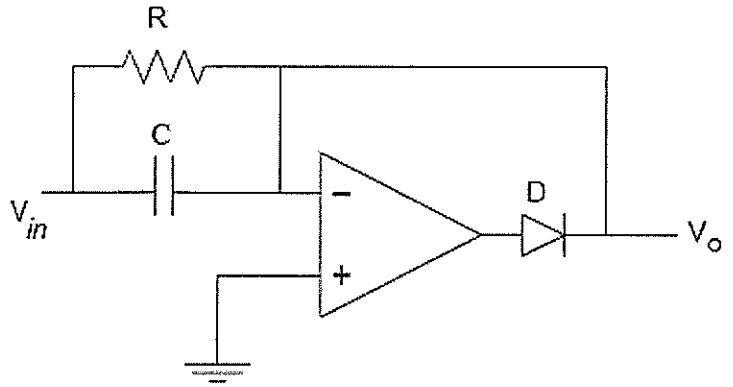

Figure Q4(c)

(i) If the input voltage $V_{in} = V_m \sin\omega t$, explain briefly the operation of the circuit and find the output voltage, Vo at various time intervals. [7 marks]

(ii) The input voltage, $V_{in} = 2 \sin\omega t$ is to be clamped to a DC level of +8V. Assuming an ideal op-amp and ±12V supply voltage, modify the circuit in Figure Q4(c) to obtain the required output. [5 marks]

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